Abstract of the Disclosure

The invention relates to a memory system which is configured with a plurality of memory controllers (SCx), disposed in parallel on a clocked bus (B), and memory chips (Fx) associated with the respective memory controllers (SCx). The system communicates via the bus (B) with a host system (HS) by means of operational memory commands using logical memory sector numbers. The inventive system is characterized in that for any memory operation requested by the host system (HS) the memory controller (SCx) affected with respect to a range of logical memory sector numbers (SCx) takes over the bus for communication with the host system (HS) by means of arbitration.